## REMARKS

The claims have been amended in view of the Office action and in view of the remarks which follow, they are believed to be in condition for allowance. The specification has been amended to clarify and elucidate written description of features shown in the drawings.

### Claim Rejections - 35 U.S.C. § 102

In section 2 of the Detailed Action, under 35 U. S. C. 102(b), claims 21-28 and 40 were rejected as being anticipated by Gilton et a1. (US Pat. 6, 143,611, hereinafter Gilton). The Office Action stated as follows:

> "Gilton discloses in figs. 5- 7 a FET device comprising: a substrate 32 with a top substrate surface upon which a gate electrode stack is formed; gate electrode stack (col. 3, line 62 through col. 4, line 1) comprising: a gate electrode 34 formed over a gate dielectric layer 33, gate dielectric layer 33 being formed on top substrate surface 32; gate electrode 34 having a top gate electrode surface and having gate electrode sidewalls; sidewall spacers 62 formed on gate electrode sidewalls aside from gate electrode 34; a cap layer 35 having outer edges and a top formed on top gate electrode surface; a hard mask 39 formed on top of cap 35; notches formed in outer edges of cap layer 35 recessed from gate electrode sidewalls; notches in outer edges of cap layer 35 being filled with protective plugs 50 formed on top of gate electrode layer 34 (col. 5, lines 11-33); and sidewall spacers 62 reaching along gate electrode sidewalls to above a level at which protective plugs 50 contact gate electrode 34 whereby sidewall spacers 62 are contiguous with and overlapping protective plugs 50 covering sidewalls of gate electrode 33 and a raised source/drain region 64 on top of said silicon layer 32 aside from spacers 62 (col. 5, lines 42-47).

It is respectfully submitted that the rejection under 35 U.S.C. § 102 is moot in view of amendments to the claims. In particular the amendments make it clear that the recess is formed in the polysilicon of the gate electrode. That is not taught by the prior art cited. In other words, it is respectfully submitted that Gilton fails to suggest that the gate electrode recess is formed in a polysilicon gate electrode. What is taught by Gilton is that a silicide layer 35 is recessed, but that the silicon layer 34 is not recessed which is the opposite of what is taught herein. The present invention is directed to solving the problem of formation of spurious growth structures upon exposed portions of the sidewalls of polysilicon gate electrodes. There is no suggestion of such a concept by Gilton in which the "notch" comprises the narrower dimension of the silicide ($WSi_2$) layer 35 above the silicon (polysilicon) layer 34 as described at Col. 3, line 62-Col 4, line 32. The ($WSi_2$) layer 35 of Gilton is recessed within the lateral edges of layers 34 and 36 by selectively faster etching rates as described at Col. 4, lines 52-63. Thus the silicon (polysilicon)

layer 34 is not notched as taught and claimed herein. Moreover, the problem of formation of spurious growth structures upon exposed portions of the sidewalls of polysilicon gate electrodes is not addressed by the references.

## Claim Rejections - 35 U.S.C. § 103

In section 3 of the Detailed Action, under 35 U.S.C. 103 (a), claims 29-39 were rejected as being unpatentable over Gilton (US Pat. 6,143,611) in view of Chang et al. (US Pat, 6,030,863, herein after Chang). The Office Action stated as follows:

> "Gilton discloses in figs. 5- 7 a FET device comprising: a substrate 32 with a top substrate surface upon which a gate electrode stack is formed; gate electrode stack (col. 3, line 62 through col. 4, line 1) comprising: a gate electrode 34 formed over a gate dielectric layer 33, gate dielectric layer 33 being formed on top substrate surface 32; gate electrode 34 having a top gate electrode surface and having gate electrode sidewalls; sidewall spacers 62 formed on gate electrode sidewalls aside from gate electrode 34; a cap layer 35 having outer edges and a top formed on top gate electrode surface; a hard mask 39 formed on top of cap 35; notches formed in outer edges of cap layer 35 recessed from gate electrode sidewalls; notches in outer edges of cap layer 35 being filled with protective plugs 50 formed on top of gate electrode layer 34 ( col. 5, lines 11-33); and sidewall spacers 62 reaching along gate electrode sidewalls to above a level at which protective plugs 50 contact gate electrode 34 whereby sidewall spacers 62 are contiguous with and overlapping protective plugs 50 covering sidewalls of gate electrode 33 and a raised source/drain region 64 on top of said silicon layer 32 aside from spacers 62 (col. 5, lines 42-47)."
>
> "Gilton fails to disclose the cap layer is an amorphous silicon layer formed of germanium and silicon ions. However, Chang teaches amorphous silicon/amorphous silicon-germanium is used for the gate electrode material ( col. 5, lines 12-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Gilton by using the gate electrode material as taught by Chang, in order to increase the conductivity of the gate electrode (See Abstract)."

First of all, the claims have been amended to make it clear that the notch is formed in the polysilicon of the gate electrode, so it is believed that the rejection if now moot for reasons explained in detail below.

Before discussing the changes to the claims, attention is called to the fact that with reference to Chang the rejection included the phrase "in order to increase the conductivity". That is believed to be a *non sequitur* with respect to the focus of the present invention. The present invention is focused upon elimination of spurious growth of silicon nodules, not "conductivity" which is not

mentioned anywhere in the present application. However the problem of spurious growth of nodules at the top of the polysilicon of a gate electrode in discussed in several paragraphs.

In paragraphs 0006 and 0008 of the published application, the problem of spurious growth of silicon nodules is described as being caused by exposure of the top of the gate polysilicon by "spacer pull down" and in paragraphs 0009 and 0010 applicants stated that the object of the present invention is to prevent this exposure. Spacer pull down is discussed in paragraph [0023] of the instant application which reads as follows:

> "[0023] FIG. 2A shows spacer pull down to the same level as FIG. 1A, but the dielectric plug 26P prevents exposure of the polysilicon of the gate electrode 18 during the step of forming the raised source/drain regions 28S/28D."

Paragraph [0006] of the instant application reads as follows:

> "[0006] The process requirement in the past has been to protect the polysilicon of the gate polysilicon 18 with spacers 16 for the purpose of avoiding the formation of spurious epitaxial growth during the raised source drain formation."

Paragraph [0008] of the instant application reads as follows:

> "[0008] The process of formation of raised source/drain regions suffers from a very limited process window. Any exposure of the gate polysilicon through either the hard mask 22 and/or above the sidewall spacers 16 results in unwanted epitaxial growth of silicon nodules 28T on the upper surfaces of the gate electrode 18 where they are exposed. "

The original abstract of the present application stated as follows

> "A method is provided for forming an SOI MOSFET device with a silicon layer formed on a dielectric layer with a gate electrode stack, with sidewall spacers on sidewalls of the gate electrode stack and raised source/drain regions formed on the surface of the silicon layer. The gate electrode stack comprises a gate electrode formed of polysilicon over a gate dielectric layer formed on the surface of the silicon layer. A plug of dielectric material is formed in a notch in a cap layer above the gate polysilicon. The sidewalls of the gate electrode is covered by the sidewall spacers which cover a portion of the plug for the purpose of eliminating the exposure of the gate polysilicon so that formation of spurious epitaxial growth during the formation of raised source/drain regions is avoided."

Paragraph [0024] of the instant application reads as follows:

> "[0024] FIG. 2B shows the device 10 of FIG. 2A after formation of the raised source/drain regions 28S/28D with the improvement that the epitaxial growth is only at the site of the source region 28S and drain regions 28D. There is no spurious growth on the top corner of the polysilicon of the gate electrode 18 of the kind seen in FIG. 1B."

APPLICANT'S NOTCH IS IN THE POLYSILICON NOT IN THE SILICIDE.

In Gilton the "notch" is not formed in the polysilicon in the top of the gate stack as it is in our invention but actually a laterally recessed silicide layer (or other material) with a different oxidation rate than the polysilicon. This clearly makes the structure in Gilton different than our structure. There is no suggestion by Gilton of forming a notch in the polysilicon. Thus the reference fails to suggest the subject matter of the amended claims.

There is no suggestion of such a concept by Gilton. In Gilton the "notch" comprises the narrower dimension of the silicide ($WSi_2$) layer 35 above the silicon (polysilicon) layer 34 as described at Col. 3, line 62-Col 4, line 32. The ($WSi_2$) layer 35 of Gilton is recessed within the lateral edges of layers 34 and 36 by selectively faster etching rates as described at Col. 4, lines 52-63. Thus the silicon (polysilicon) layer 34 is not notched as taught and claimed herein. Moreover, the problem of formation of spurious growth structures upon exposed portions of the sidewalls of polysilicon gate electrodes is not addressed by the references.

No fee is believed to be due for the submission of this amendment. If any fees are required, however, please charge such fees to Deposit Account No. 09-0458.

In view of the amendments and the above remarks favorable action including allowance of the claims and the application as a whole are respectfully solicited.

Respectfully submitted,


Graham S. Jones, II, Attorney
Reg. No. 20,429

Telephone (845) 473-9118 FAX (845) 485-9399